EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 10233687
PUBLICATION DATE : 02-09-98

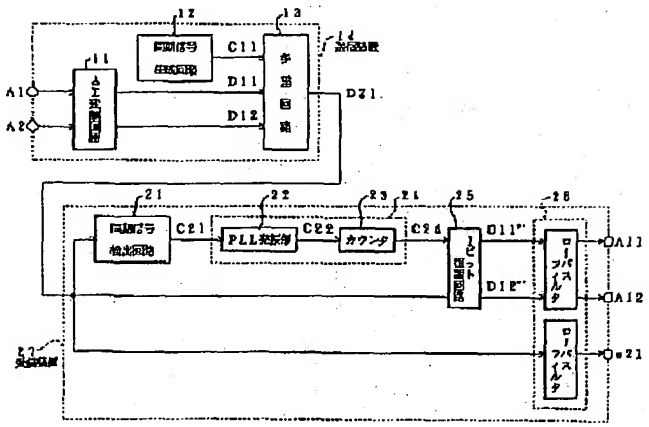
APPLICATION DATE : 20-02-97
APPLICATION NUMBER : 09036749

APPLICANT : SHARP CORP;

INVENTOR : INOTSUKA YUKINORI;

INT.CL. : H03M 3/02 H04J 3/00

TITLE : SIGNAL TRANSMITTER



ABSTRACT : PROBLEM TO BE SOLVED: To improve the economy by simplifying the entire configuration of the signal transmitter.

SOLUTION: A ΔΣ modulation circuit 11 of a transmitter 14 converts analog signals A, A2 into 1-bit digital signals D11, D12, and a multiplexer circuit 13 applies time division multiplex to the signals D11, D12 and a synchronizing signal clock C11 and the multiplexed signal D21 is transmitted to a receiver 27. A 1-bit demodulation circuit 25 demodulates the multiplexed digital signal D21 based on the synchronizing signal detected by a synchronizing signal detection circuit 21 from the received multiplexed digital signal D21 in a timing in response to each system. Each demodulated signal is converted into analog signals A11, A12 by a low pass filter 26.

CLAIMS

[Claim(s)]
[Claim 1] In the signal-transmission equipment which transmits and receives two or more digital signals in a transmitting side The signal transformation section which changes two or more input signals into a 1-bit digital signal, It has the multiplex section which carries out multiplex [of the synchronizing signal generation section which generates a synchronizing signal, and the above-mentioned 1 bit digital signal and the above-mentioned synchronizing signal] to one digital signal for transmission, and transmits. In a receiving side The synchronizing signal detecting element which detects the above-mentioned synchronizing signal from the received above-mentioned digital signal for transmission, The clock generation section which generates the clock which synchronized with the above-mentioned digital signal for transmission from the above-mentioned synchronizing signal, Signal-transmission equipment characterized by having the 1-bit recovery section which restores to the above-mentioned digital signal for transmission to the timing according to each system of the above-mentioned input signal, respectively based on the above-mentioned clock.
[Claim 2] Signal-transmission equipment according to claim 1 characterized by having the low pass filter into which the above-mentioned digital signal for transmission is inputted as it is, without separating the digital signal of each system of the above-mentioned input signal from the received above-mentioned digital signal for transmission by the receiving side.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the signal-transmission equipment which transmits efficiently the digital signal by the 1-bit coding method obtained by a delta sigma modulation etc.
[0002]
[Description of the Prior Art] Conventionally, in case a digital signal is transmitted between digital instruments, the various transmission approaches are used. As the transmission approach currently used widely, the parallel transmission approach of transmitting the digital signal of each system by the respectively different transmission system, and the serial transmission approach of transmitting two or more digital signals of a system by carrying out time sharing of the one transmission system are mentioned, for example.
[0003] Said serial transmission approach is an approach of carrying out time sharing of the one transmission system, and transmitting the divided digital signal of a system which corresponds for every time amount. In this approach, a receive section needs to judge whether the digital signal transmitted in a transmission system is equivalent to the digital signal of which system, and the special format for it is performed. Therefore, the processing in the transmitting section and a receive section becomes complicated. Furthermore, since it is necessary to distinguish this information and a digital signal to transmit information required for the decision concerned by said transmission system, the processing in the transmitting section and a receive section becomes still more complicated.
[0004] Therefore, the transmission system of dedication is assigned to the digital signal of each system, respectively and the parallel transmission approach transmitted as it is is used for it in many cases to simplify the configuration of the transmitting section and a receive section. Moreover, the digital signal transmission approach of transmitting two or more digital signals to parallel by the transmission system for the number of bits encoded to several bits is also performed.
[0005]
[Problem(s) to be Solved by the Invention] However, in the digital signal transmission approach by the conventional parallel transmission approach, the transmission system of only the number of the systems of a digital signal or the encoded transmission system for the number of bits is needed. Furthermore, when the digital signal of each system synchronizes with a data clock, it is necessary to transmit the data clock concerned by another transmission system. Therefore, it is difficult to reduce the number of transmission systems. Since each transmission system is equipped with the transmitting section, a receive section, the transmission line, etc., the increment in such a transmission system has the trouble of inviting complication and enlargement of the configuration of the whole transmission means.
[0006] On the other hand, in order that the digital signal by which time sharing was carried out may judge of which system it is a digital signal in a serial transmission system in a receive section, respectively, it is necessary to perform a special format to this digital signal, and has the trouble that the configuration of the transmitting section and a receive section becomes complicated.
[0007]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, signal-transmission equipment according to claim 1 In the signal-transmission equipment which transmits and receives two or more digital signals in a transmitting side The signal transformation section which changes two or more input signals into a 1-bit digital signal, It has the multiplex section which carries out multiplex [of the synchronizing signal generation section which generates a synchronizing signal, and the above-mentioned 1 bit digital signal and the

above-mentioned synchronizing signal] to one digital signal for transmission, and transmits. In a receiving side The synchronizing signal detecting element which detects the above-mentioned synchronizing signal from the received above-mentioned digital signal for transmission, It is characterized by having the clock generation section which generates the clock which synchronized with the above-mentioned digital signal for transmission from the above-mentioned synchronizing signal, and the 1-bit recovery section which restores to the above-mentioned digital signal for transmission to the timing according to each system of the above-mentioned input signal based on the above-mentioned clock, respectively.

[0008] When two or more analog signals are inputted into a transmitting side by the above-mentioned configuration, it is changed into a 1-bit digital signal by the signal transformation section like deltasigma modulation circuit, respectively. And Time Division Multiplexing of the two or more 1-bit digital signal is carried out to the synchronizing signal generated in a simple circuit, and it is transmitted as one digital signal for transmission.

[0009] At a receiving side, the above-mentioned synchronizing signal is detected in a simple circuit, and the above-mentioned digital signal for transmission is recovered from the above-mentioned digital signal for transmission to the timing according to each above-mentioned system based on the detected above-mentioned synchronizing signal, respectively.

[0010] That is, for example, while synchronizing with the digital signal for transmission based on the above-mentioned synchronizing signal, a data clock with the same frequency as the digital signal for transmission is generated. And the high-speed clock of the frequency of the integral multiple of the data clock is generated. Based on this high-speed clock, it restores to the above-mentioned digital signal for transmission to the timing according to each above-mentioned system, respectively.

[0011] By changing into an analog signal the signal to which it restored with a low pass filter, an analog output signal can be taken out by the receiving side.

[0012] When the digital signal of two or more multi-bits is inputted into a transmitting side, it is similarly changed into a 1-bit digital signal by the above-mentioned signal transformation section, respectively.

[0013] Therefore, unlike the digital signal transmission approach by the conventional parallel transmission approach, the number of transmission systems one, and the transmission system of only the number of the systems of a digital signal or the encoded transmission system for the number of bits is unnecessary. Moreover, it is not necessary to transmit a data clock by another transmission system. Therefore, it is possible to reduce the number of transmission systems. Since each transmission system is equipped with the transmitting section, a receive section, the transmission line, etc., by controlling the increment in such a transmission system, it can simplify the configuration of the whole transmission means and can prevent enlargement.

[0014] When the digital signal by which time sharing was carried out, on the other hand, judges by the receiving side of which system it is a digital signal, respectively unlike the conventional serial transmission system, it is not necessary to perform a special format to the digital signal, and transmission and reception are possible with a simple configuration.

[0015] Therefore, moreover, two or more signals can be transmitted by simple circuitry using one digital signal. So, the configuration of the whole signal-transmission equipment can be simplified and profitability can be raised.

[0016] In addition to the configuration of claim 1, signal-transmission equipment according to claim 2 is a receiving side, and is characterized by having the low pass filter into which the above-mentioned digital signal for transmission is inputted as it is, without separating the digital signal of each system of the above-mentioned input signal from the received above-mentioned digital signal for transmission.

[0017] By the above-mentioned configuration, if the above-mentioned digital signal for transmission is made to pass the above-mentioned low pass filter, since the section of a synchronizing signal of "H" is the same as the section of "L", the potential which is 0 volt shall be held. Therefore, it is equalized with 1-bit digital signals other than a synchronizing signal. So, the output of a monophonic signal can be obtained.

[0018]

[Embodiment of the Invention] It will be as follows if one gestalt of operation of this invention is explained based on drawing 1 and drawing 2 . Here, two analog signals are transmitted. The signal-transmission equipment concerning the gestalt of this operation has the sending set 14 and the receiving set 27, as shown in drawing 1 .

[0019] A sending set 14 has the deltasigma (delta sigma) modulation circuit (signal transformation section) 11,

the synchronizing signal generation circuit (synchronizing signal generation section) 12, and a multiplex circuit (multiplex section) 13. The deltasigma modulation circuit 11 changes and outputs an analog signal to a 1-bit digital signal. The synchronizing signal generation circuit 12 generates the 3 times as many clock C11 as the data clock of this 1-bit digital signal. A multiplex circuit 13 carries out multiplex [of a 1-bit digital signal and the clock C11].

[0020] A receiving set 27 has the synchronizing signal detector (synchronizing signal detecting element) 21, the 24 or 1 bit (clock generation section) demodulator circuit (1-bit recovery section) 25 of PLL circuits, and a low pass filter 26. The synchronizing signal detector 21 detects a synchronizing signal like the after-mentioned from an input signal. The PLL circuit 24 has the PLL oscillation section 22 which oscillates the high-speed clock C22 of the integral multiple (here 8 times) of the clock inputted, and the counter 23 counted in falling of the clock C22 inputted, and outputs a clock C24 from a counter 23. The 1-bit demodulator circuit 25 restores to it and outputs a 1-bit digital signal from an input digital signal in the standup or falling of the clock C24 inputted.

[0021] First, two analog signals, A1 and A2, are inputted into a sending set 14, respectively. [i.e.,] Then, an analog signal is changed into the 1-bit digital signals D11 and D12 in the deltasigma modulation circuit 11, and is inputted into a multiplex circuit 13. Here, the 1-bit digital signals D11 and D12 turn into a synchronizing signal in the synchronizing signal generation circuit 12 by generating the 3 times as many clock C11 as the data clock of a 1-bit digital signal, and carrying out multiplex to the 1-bit digital signals D11 and D12 by the multiplex circuit 13 so that they may interchange and may not be outputted with a receiving set 27 after transmission. Thus, the multiplexing digital signal D21 (digital signal for transmission) is acquired.

[0022] The multiplexing digital signal D21 is inputted into a receiving set 27, it is the synchronizing signal detector 21, and detects the minimum"H" section, i.e., "H" section of a synchronizing signal, and generates the clock C21 which takes binary [for every falling of a synchronizing signal / different].

[0023] The PLL circuit 24 oscillates the 8 times as many clock C22 as a clock C21 by the PLL oscillation section 22. And a clock C24 is obtained with the counter 23 counted in falling of an input clock. This clock C24 and the multiplexing digital signal D21 are inputted into the 1-bit demodulator circuit 25, the multiplexing digital signal D21 is read in the standup of a clock C24, and 1-bit digital signal D11' is outputted. Outputted D11' is read once again in falling of a clock C24, and 1-bit digital signal D11" is outputted.

[0024] Moreover, the multiplexing digital signal D21 is read in falling of a clock C24, and 1-bit digital signal D12" is outputted.

[0025] therefore -- said -- one -- a bit -- a demodulator circuit -- 25 -- a sending set -- 14 -- delta -- sigma -- a modulation circuit -- 11 -- an output -- D -- 11 -- D -- 12 -- almost -- being equivalent -- one -- a bit -- a digital signal -- D -- 11 -- " -- D -- 12 -- " -- it can get over .

[0026] and -- one -- a bit -- a demodulator circuit -- 25 -- obtaining -- having -- one -- a bit -- a digital signal -- D -- 11 -- " -- D -- 12 -- " -- a low pass filter -- 26 -- passing -- making -- analog signals A11 and A12 -- getting over .

[0027] If it inputs into a low pass filter 26 as it is, since the section of a synchronizing signal of "H" is the same as the section of "L", the multiplexing digital signal D21 treated as a transmission signal of this invention will have the potential which is 0 volt held, will be equalized with 1-bit digital signals other than a synchronizing signal, and will be outputted as a monophonic signal (a21).

[0028] In addition, although each technique indicated by JP,6-66138,A and JP,6-85683,A has described the multiplex approach of a 1-bit signal, the art after transmission is not described. After carrying out multiplex and transmitting, this invention judges of which system it is an input signal (for example, stereo audio signals Lch and Rch), and in case it gets over, in order to be able to perform this decision in a simple circuit, as the synchronizing signal was described above, it is carrying out multiplex. [it]

[0029]

[Effect of the Invention] As mentioned above, the signal-transmission equipment of this invention according to claim 1 In the signal-transmission equipment which transmits and receives two or more digital signals in a transmitting side The signal transformation section which changes two or more input signals into a 1-bit digital signal, It has the multiplex section which carries out multiplex [of the synchronizing signal generation section which generates a synchronizing signal, and the above-mentioned 1 bit digital signal and the above-mentioned synchronizing signal] to one digital signal for transmission, and transmits. In a receiving side The synchronizing signal detecting element which detects the above-mentioned synchronizing signal from the received above-mentioned digital signal for transmission, It is the configuration of having the clock generation

section which generates the clock which synchronized with the above-mentioned digital signal for transmission from the above-mentioned synchronizing signal, and the 1-bit recovery section which restores to the above-mentioned digital signal for transmission to the timing according to each system of the above-mentioned input signal based on the above-mentioned clock, respectively.

[0030] So, the configuration of the whole signal-transmission equipment is simplified and the effectiveness that profitability can be raised is done.

[0031] The signal-transmission equipment of this invention according to claim 2 is the configuration of having the low pass filter into which the above-mentioned digital signal for transmission is inputted as it is, without separating the digital signal of each system of the above-mentioned input signal from the above-mentioned digital signal for transmission which in addition to the configuration of claim 1 is a receiving side and was received.

[0032] So, in addition to the effectiveness by the configuration of claim 1, the effectiveness that the output of a monophonic signal can be obtained is done.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to the signal-transmission equipment which transmits efficiently the digital signal by the 1-bit coding method obtained by a delta sigma modulation etc.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, in case a digital signal is transmitted between digital instruments, the various transmission approaches are used. As the transmission approach currently used widely, the parallel transmission approach of transmitting the digital signal of each system by the respectively different transmission system, and the serial transmission approach of transmitting two or more digital signals of a system by carrying out time sharing of the one transmission system are mentioned, for example.

[0003] Said serial transmission approach is an approach of carrying out time sharing of the one transmission system, and transmitting the divided digital signal of a system which corresponds for every time amount. In this approach, a receive section needs to judge whether the digital signal transmitted in a transmission system is equivalent to the digital signal of which system, and the special format for it is performed. Therefore, the processing in the transmitting section and a receive section becomes complicated. Furthermore, since it is necessary to distinguish this information and a digital signal to transmit information required for the decision concerned by said transmission system, the processing in the transmitting section and a receive section becomes still more complicated.

[0004] Therefore, the transmission system of dedication is assigned to the digital signal of each system, respectively and the parallel transmission approach transmitted as it is is used for it in many cases to simplify the configuration of the transmitting section and a receive section. Moreover, the digital signal transmission approach of transmitting two or more digital signals to parallel by the transmission system for the number of bits encoded to several bits is also performed.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, signal-transmission equipment of this invention according to claim 1, In the signal-transmission equipment which transmits and receives two or more digital signals in a transmitting side The signal transformation section which changes two or more input signals into a 1-bit digital signal, It has the multiplex section which carries out multiplex [of the synchronizing signal generation section which generates a synchronizing signal, and the above-mentioned 1 bit digital signal and the above-mentioned synchronizing signal] to one digital signal for transmission, and transmits. In a receiving side The synchronizing signal detecting element which detects the above-mentioned synchronizing signal from the received above-mentioned digital signal for transmission, It is the configuration of having the clock generation section which generates the clock which synchronized with the above-mentioned digital signal for transmission from the above-mentioned synchronizing signal, and the 1-bit recovery section which restores to the above-mentioned digital signal for transmission to the timing according to each system of the above-mentioned input signal based on the above-mentioned clock, respectively.
[0030] So, the configuration of the whole signal-transmission equipment is simplified and the effectiveness that profitability can be raised is done.
[0031] The signal-transmission equipment of this invention according to claim 2 is the configuration of having the low pass filter into which the above-mentioned digital signal for transmission is inputted as it is, without separating the digital signal of each system of the above-mentioned input signal from the above-mentioned digital signal for transmission which in addition to the configuration of claim 1 is a receiving side and was received.
[0032] So, in addition to the effectiveness by the configuration of claim 1, the effectiveness that the output of a monophonic signal can be obtained is done.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in the digital signal transmission approach by the conventional parallel transmission approach, the transmission system of only the number of the systems of a digital signal or the encoded transmission system for the number of bits is needed. Furthermore, when the digital signal of each system synchronizes with a data clock, it is necessary to transmit the data clock concerned by another transmission system. Therefore, it is difficult to reduce the number of transmission systems. Since each transmission system is equipped with the transmitting section, a receive section, the transmission line, etc., the increment in such a transmission system has the trouble of inviting complication and enlargement of the configuration of the whole transmission means.

[0006] On the other hand, in order that the digital signal by which time sharing was carried out may judge of which system it is a digital signal in a serial transmission system in a receive section, respectively, it is necessary to perform a special format to this digital signal, and has the trouble that the configuration of the transmitting section and a receive section becomes complicated.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, signal-transmission equipment according to claim 1 In the signal-transmission equipment which transmits and receives two or more digital signals in a transmitting side The signal transformation section which changes two or more input signals into a 1-bit digital signal, It has the multiplex section which carries out multiplex [of the synchronizing signal generation section which generates a synchronizing signal, and the above-mentioned 1 bit digital signal and the above-mentioned synchronizing signal] to one digital signal for transmission, and transmits. In a receiving side The synchronizing signal detecting element which detects the above-mentioned synchronizing signal from the received above-mentioned digital signal for transmission, It is characterized by having the clock generation section which generates the clock which synchronized with the above-mentioned digital signal for transmission from the above-mentioned synchronizing signal, and the 1-bit recovery section which restores to the above-mentioned digital signal for transmission to the timing according to each system of the above-mentioned input signal based on the above-mentioned clock, respectively.

[0008] When two or more analog signals are inputted into a transmitting side by the above-mentioned configuration, it is changed into a 1-bit digital signal by the signal transformation section like deltasigma modulation circuit, respectively. And Time Division Multiplexing of the two or more 1-bit digital signal is carried out to the synchronizing signal generated in a simple circuit, and it is transmitted as one digital signal for transmission.

[0009] At a receiving side, the above-mentioned synchronizing signal is detected in a simple circuit, and the above-mentioned digital signal for transmission is recovered from the above-mentioned digital signal for transmission to the timing according to each above-mentioned system based on the detected above-mentioned synchronizing signal, respectively.

[0010] That is, for example, while synchronizing with the digital signal for transmission based on the above-mentioned synchronizing signal, a data clock with the same frequency as the digital signal for transmission is generated. And the high-speed clock of the frequency of the integral multiple of the data clock is generated. Based on this high-speed clock, it restores to the above-mentioned digital signal for transmission to the timing according to each above-mentioned system, respectively.

[0011] By changing into an analog signal the signal to which it restored with a low pass filter, an analog output signal can be taken out by the receiving side.

[0012] When the digital signal of two or more multi-bits is inputted into a transmitting side, it is similarly changed into a 1-bit digital signal by the above-mentioned signal transformation section, respectively.

[0013] Therefore, unlike the digital signal transmission approach by the conventional parallel transmission approach, the number of transmission systems one, and the transmission system of only the number of the systems of a digital signal or the encoded transmission system for the number of bits is unnecessary. Moreover, it is not necessary to transmit a data clock by another transmission system. Therefore, it is possible to reduce the number of transmission systems. Since each transmission system is equipped with the transmitting section, a receive section, the transmission line, etc., by controlling the increment in such a transmission system, it can simplify the configuration of the whole transmission means and can prevent enlargement.

[0014] When the digital signal by which time sharing was carried out, on the other hand, judges by the receiving side of which system it is a digital signal, respectively unlike the conventional serial transmission system, it is not necessary to perform a special format to the digital signal, and transmission and reception are possible with a simple configuration.

[0015] Therefore, moreover, two or more signals can be transmitted by simple circuitry using one digital signal.

So, the configuration of the whole signal-transmission equipment can be simplified and profitability can be raised.
[0016] In addition to the configuration of claim 1, signal-transmission equipment according to claim 2 is a receiving side, and is characterized by having the low pass filter into which the above-mentioned digital signal for transmission is inputted as it is, without separating the digital signal of each system of the above-mentioned input signal from the received above-mentioned digital signal for transmission.
[0017] By the above-mentioned configuration, if the above-mentioned digital signal for transmission is made to pass the above-mentioned low pass filter, since the section of a synchronizing signal of "H" is the same as the section of "L", the potential which is 0 volt shall be held. Therefore, it is equalized with 1-bit digital signals other than a synchronizing signal. So, the output of a monophonic signal can be obtained.
[0018]
[Embodiment of the Invention] It will be as follows if one gestalt of operation of this invention is explained based on drawing 1 and drawing 2 . Here, two analog signals are transmitted. The signal-transmission equipment concerning the gestalt of this operation has the sending set 14 and the receiving set 27, as shown in drawing 1 .
[0019] A sending set 14 has the deltasigma (delta sigma) modulation circuit (signal transformation section) 11, the synchronizing signal generation circuit (synchronizing signal generation section) 12, and a multiplex circuit (multiplex section) 13. The deltasigma modulation circuit 11 changes and outputs an analog signal to a 1-bit digital signal. The synchronizing signal generation circuit 12 generates the 3 times as many clock C11 as the data clock of this 1-bit digital signal. A multiplex circuit 13 carries out multiplex [of a 1-bit digital signal and the clock C11].
[0020] A receiving set 27 has the synchronizing signal detector (synchronizing signal detecting element) 21, the 24 or 1 bit (clock generation section) demodulator circuit (1-bit recovery section) 25 of PLL circuits, and a low pass filter 26. The synchronizing signal detector 21 detects a synchronizing signal like the after-mentioned from an input signal. The PLL circuit 24 has the PLL oscillation section 22 which oscillates the high-speed clock C22 of the integral multiple (here 8 times) of the clock inputted, and the counter 23 counted in falling of the clock C22 inputted, and outputs a clock C24 from a counter 23. The 1-bit demodulator circuit 25 restores to it and outputs a 1-bit digital signal from an input digital signal in the standup or falling of the clock C24 inputted.
[0021] First, two analog signals, A1 and A2, are inputted into a sending set 14, respectively. [i.e.,] Then, an analog signal is changed into the 1-bit digital signals D11 and D12 in the deltasigma modulation circuit 11, and is inputted into a multiplex circuit 13. Here, the 1-bit digital signals D11 and D12 turn into a synchronizing signal in the synchronizing signal generation circuit 12 by generating the 3 times as many clock C11 as the data clock of a 1-bit digital signal, and carrying out multiplex to the 1-bit digital signals D11 and D12 by the multiplex circuit 13 so that they may interchange and may not be outputted with a receiving set 27 after transmission. Thus, the multiplexing digital signal D21 (digital signal for transmission) is acquired.
[0022] The multiplexing digital signal D21 is inputted into a receiving set 27, it is the synchronizing signal detector 21, and detects the minimum"H" section, i.e., "H" section of a synchronizing signal, and generates the clock C21 which takes binary [for every falling of a synchronizing signal / different].
[0023] The PLL circuit 24 oscillates the 8 times as many clock C22 as a clock C21 by the PLL oscillation section 22. And a clock C24 is obtained with the counter 23 counted in falling of an input clock. This clock C24 and the multiplexing digital signal D21 are inputted into the 1-bit demodulator circuit 25, the multiplexing digital signal D21 is read in the standup of a clock C24, and 1-bit digital signal D11' is outputted. Outputted D11' is read once again in falling of a clock C24, and 1-bit digital signal D11" is outputted.
[0024] Moreover, the multiplexing digital signal D21 is read in falling of a clock C24, and 1-bit digital signal D12" is outputted.
[0025] therefore -- said -- one -- a bit -- a demodulator circuit -- 25 -- a sending set -- 14 -- delta -- sigma -- a modulation circuit -- 11 -- an output -- D -- 11 -- D -- 12 -- almost -- being equivalent -- one -- a bit -- a digital signal -- D -- 11 -- " -- D -- 12 -- " -- it can get over .
[0026] and -- one -- a bit -- a demodulator circuit -- 25 -- obtaining -- having -- one -- a bit -- a digital signal -- D -- 11 -- " -- D -- 12 -- " -- a low pass filter -- 26 -- passing -- making -- analog signals A11 and A12 -- getting over .
[0027] If it inputs into a low pass filter 26 as it is, since the section of a synchronizing signal of "H" is the same as the section of "L", the multiplexing digital signal D21 treated as a transmission signal of this invention will

have the potential which is 0 volt held, will be equalized with 1-bit digital signals other than a synchronizing signal, and will be outputted as a monophonic signal (a21).
[0028] In addition, although each technique indicated by JP,6-66138,A and JP,6-85683,A has described the multiplex approach of a 1-bit signal, the art after transmission is not described. After carrying out multiplex and transmitting, this invention judges of which system it is an input signal (for example, stereo audio signals Lch and Rch), and in case it gets over, in order to be able to perform this decision in a simple circuit, as the synchronizing signal was described above, it is carrying out multiplex. [it]

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the example of 1 configuration of the signal-transmission equipment concerning this invention.
[Drawing 2] It is the timing chart of the signal treated with the configuration of drawing 1 .
[Description of Notations]
11 DeltaSigma Modulation Circuit (Signal Transformation Section)
12 Synchronizing Signal Generation Circuit (Synchronizing Signal Generation Section)
13 Multiplex Circuit (Multiplex Section)
14 Sending Set
21 Synchronizing Signal Detector (Synchronizing Signal Detecting Element)
22 PLL Oscillation Section
23 Counter
24 PLL Circuit (Clock Generation Section)
25 1-Bit Demodulator Circuit (1-Bit Recovery Section)
26 Low Pass Filter
27 Receiving Set
A1, A2, A11, A12, a21 Analog signal
C11, C21, C22, C24 Clock
D11, D12, D11", D11', and D12 -- " -- 1-bit digital signal
D21 Multiplexing digital signal (digital signal for transmission)

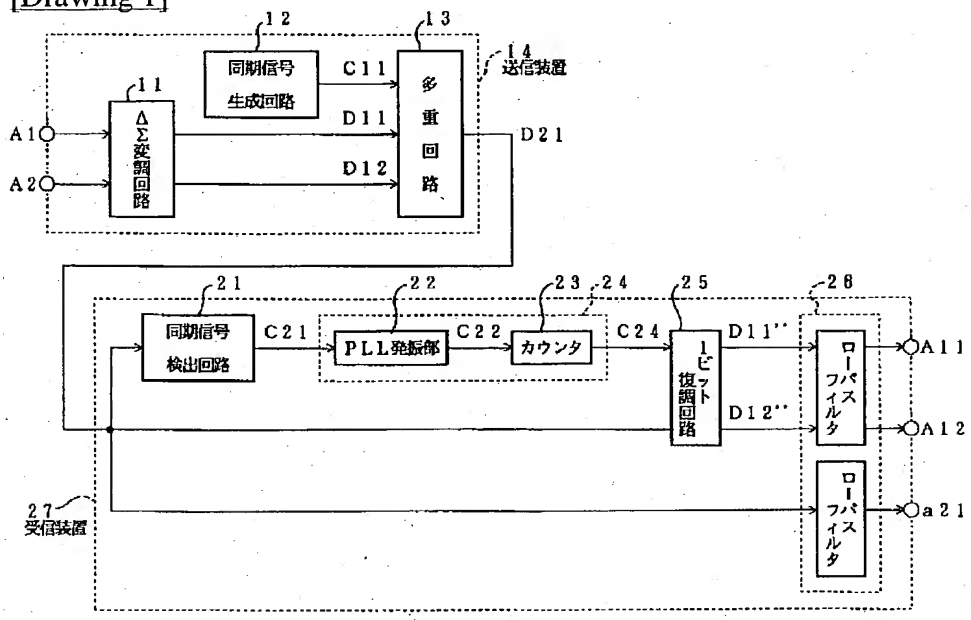
[Translation done.]

* NOTICES *

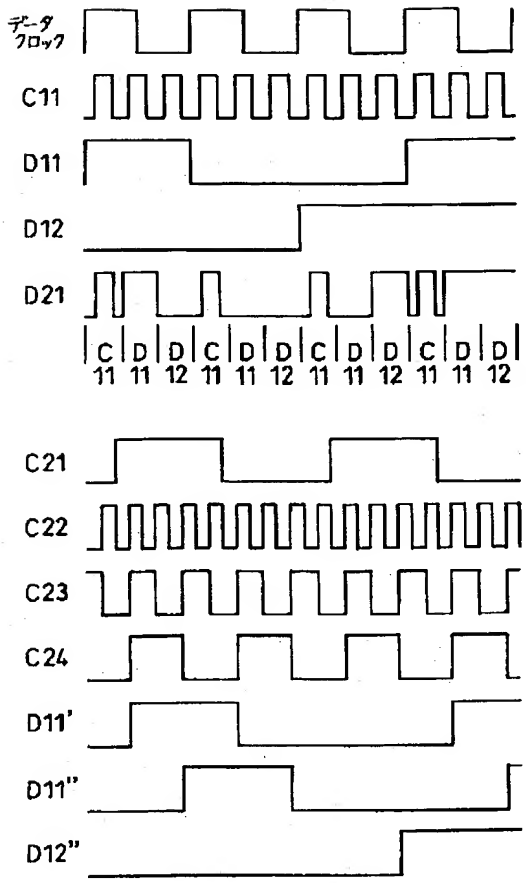
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]



[Drawing 2]



[Translation done.]